REMARKS

Claims 1-20 are pending, with claims 1 and 6 being independent. Reconsideration and allowance of the above-referenced application are respectfully requested.

Rejections under 35 U.S.C. 103

Claims 1-8 and 11-16 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over U.S. Patent No. 6,327,273 issued to Van der Putten et al. (herein after "Van der Putten") in view of U.S. Patent No. 5,062,124 issued to Hayashi et al. (hereinafter "Hayashi").

Claims 9-10 and 17-20 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Van der Putten in view of Hayashi and further in view of U.S. Patent No. 5,846,248 issued to Rokugo (hereinafter "Rokugo"). These contentions are respectfully traversed.

Initially, as noted in the previous response, the subject matter as claimed in claims 1 and 6 is a system and method for transmitting data from a source module to a terminating module over a network comprising a plurality of modules, in which each of the modules in the network operate with an **independent, non-synchronized**, clock. The terminating module is synchronized to the clock of the source module using the accumulated phase difference, which is transmitted over the network to the terminating module. The accumulated phase difference is the difference between the input and output of each of the modules through which the data is transmitted. The terminating module receives all the accumulated phases differences and uses them to lock an output clock with the input clock of the source module. The claimed subject matter allows synchronous data to be transmitted over a network, **without requiring each of the modules in the network to be synchronized to one another**.

Van der Putten

Van Der Putten relates to transmitting a network clock signal over a network which is internally synchronized to a different timing signal (see column 1, lines 20 to 25). Rather than the network clock signal being transmitted, the transmitter transmits a phase difference (P)

between the network clock signal (CLK 2) and the transmitter clock (CLK 1). The phase difference is used at the receiver (RX) together with the receiver clock (CLK1') to reconstruct the network clock signal (CLK2). This is possible because the transmitter clock (CLK1) and receiver clock (CLK1') are synchronized. This is clearly described in column 2, lines 45 to 63.

Therefore, a clear requirement of the system of Van der Putten is that each module in the network (i.e. transmitter and receiver modules TX and RX) has a clock (CLK1, CLK1') that is synchronized with the clocks of the other modules in the network. If the transmitter clock CLK1 were not synchronized with the receiver clock CLK1', the network clock signal CLK2 could not be determined at the receiver.

Thus, there is a clear difference between the teaching of Van Der Putten and the claimed subject matter that has not been recognized by the Examiner. That difference is that the network modules in Van der Putten must each be synchronized with one another. In contrast, the claimed subject matter does not require that each of the modules in the network be synchronized with one another. The benefit of the claimed subject matter is that it is possible to transmit a synchronous signal over a network without requiring each of the modules in the network to be synchronized to one another.

A further distinction not recognized by the Examiner is that Van der Putten is silent regarding determining a phase difference between the input clock and the output clock of each of modules in the network, which is requirement of claims 1 and 6 of the present application. In Van der Putten the receiver RX does not calculate a phase difference between the input signal and CLK'. It simply combines the phase difference P with CLK' to generate CLK'. That is not a calculation of the phase difference between the input and the output.

Hayashi

Hayashi discloses a system for synchronizing the master clock of a first communication system with a reference clock supplied by a signal from an external communication system. Within the first communication system there is a master clock, so that each module within the communication system is synchronized with other modules. When the first communication system is connected to an outside data network it receives data that uses a reference clock, which

is different from the master clock of the first communication system. Thus, the system described in Hayashi is used to synchronize the master clock of the first communication system with the reference clock received from the external network.

This is accomplished by the device I1, which is connected to the external network calculating a phase difference between the reference clock from the external network and the master clock of the first communication system. This calculated phase difference is sent to device I2, which contains the master clock oscillator. The master clock oscillator is then adjusted based on the phase difference received from device I1 to match the phase of the reference clock.

It is clear that in the system of Hayashi each of the modules within the communications system are synchronized with each other as they use the same master clock. The inputs and outputs of each module are also synchronized with the master clock. It is only the input from the external network that is not synchronized initially. However, subsequent to adjustment of the master clock all of the inputs and outputs of the communication system are synchronized with one another.

In sharp contrast, claim 1 of the present application requires that each of the modules in a network have outputs that are not synchronized with the input to the module. That is clearly not the case in the system disclosed in Hayashi. Claim 1 also requires that each module in the network operates with a clock that is not synchronized with the clocks of the other modules in the network. Again, this is clearly not the case in Hayashi. Claim 1 also requires determining a phase difference between the input clock and the output clock of each module (and there are a plurality of them) and transmitting that accumulated phase difference to the terminating module in the network. Again that is clearly not disclosed in Hayashi.

Combination of Van der Putten with Hayashi

It is clear that neither Van der Putten nor Hayashi discloses transmitting signal over a network in which each of the modules in the network is not synchronized with the other modules. In both Van der Putten and Hayashi it is a requirement that all the modules in the

network are synchronized to one another. Accordingly, it is clear that the combination of Van der Putten with Hayashi would not result in the subject matter claimed in claims 1 and 6.

Furthermore, neither Van der Putten nor Hayashi discloses determining a phase difference between the input clock and the output clock of each module in the network, and provide no motivation to do so.

Contrary to the Office's contention, the cited portions of Van der Putten do not disclose the requirements of claims 1 and 6. For example, Examiner's statement that column 4, lines 29 to 36 and lines 43 to 48 of Van der Putten disclose that the "transmitter module reference clock and receiver module reference clock are not synchronized with each other" is respectfully traversed.

In particular, Column 4, lines 29 to 36 of Van der Putten states:

> "...EMBED are interconnected. The transmitter TX in the figure further contains an unlabelled star shaped device which may represent any kind of means which transforms the transmit clock signal CLK1 into a reference signal R. The reference signal R is thus nothing but a transformed clock signal CLK1, is synchronous with this clock signal CLK1 and is applied to inputs of the data embedder EMBED and phase ...".

Contrary to the Examiner's assertion, there is no mention in this passage of the transmit clock CLK1 and receiver clock CLK1' not being synchronized with one another.

Further, Column 4, lines 43 to 48 of Van der Putten states:

> "...receive clock input CLK1' and output connected to the network clock output CLK2' of the receiver RX. A similar star shaped, unlabelled device is drawn in the receiver RX to represent any kind of means e.g. a sequence of frequency dividers, which transforms the receive clock signal CLK1' into a reference signal R' similar to the transformation in the...".

Again, contrary to the Examiner's assertion, there is no disclosure of transmit clock CLK1 and receiver clock CLK1' not being synchronized with each other. The teaching of Van der Putten is very clear in this regard. The clocks of each module in the network must be synchronized with each other. This is made absolutely clear in the abstract, in column 1, lines 57 to 63 and in column 2, lines 45 to 53.

The Examiner has referred to the diagram in Van der Putten, alleging that it shows that each of the plurality of modules in the network has a single input, referring specifically to receiver module RX. However, it is clear from the diagram that the transmitter module TX has more than a single input, but only a single output.

The Examiner has referred to column 2, lines 45 to 53 as disclosing that the outputs of each module are phase locked to each other but are not synchronized with respect to the input. Again we respectfully disagree. This passage states that the transmit module clock signal and receive module clock signal are synchronized i.e. the clock signals of each module are synchronized with one another. It makes no reference to whether the input from TL is synchronized with the outputs DATA' and CLK2'. Nor does it refer to whether DATA' and CLK2' are phase locked to each other.

The Examiner's contention that Van der Putten discloses transmitting an **accumulated** phase difference is further respectfully traversed. Since in Van der Putten all of the modules (TX and RX) are synchronized, there is no accumulated phase difference between the input and output of each module.

Independent Claim 6 recites similar features as Claim 1 and is also patentably distinguishable over the proposed Van der Putten-Hayashi combination for analogous reasons to those discussed for independent Claim 1.

Additionally, claims 2-5, 7-8, 11-16 depend generally from independent Claims 1 or 6; these dependent claims are patentably distinguishable over Van der Putten or Hayashi, either alone or in combination, for at least the reasons provided above.

Furthermore, claims 9-10 and 17-20 also depend generally from independent Claims 1 or 6; these dependent claims are patentably distinguishable over Van der Putten, Hayashi, or Rokugo, either alone or in combination, for at least the reasons provided above.

Thus, all the pending claims are allowable for at least the reasons provided above.

The foregoing comments made with respect to the positions taken by the Examiner are not to be construed as acquiescence with other positions of the Examiner that have not been explicitly contested. Accordingly, the above arguments for patentability of a claim should not be

construed as implying that there are not other valid reasons for patentability of that claim or other claims.

Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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